Lab 1 Specifications

The focus of lab 1 specifications, in addition to proving hardware functionality, is correct Verilog hierarchy and style. Block diagram and schematic specifications will be checked in more detail in later labs, but don't cut corners on them because you need feedback of your first attempts before you are graded on them for real.

Hardware Specifications

Proficiency

- ☐ Development board is fully assembled (e.g., all parts soldered)
- ☐ Verilog module to control LEDs and a 7-segment display written
- ☐ FPGA programmed with Verilog code.
- ☐ 7-segment display can display all sixteen hexadecimal digits from `0x0` through `0xF`
- ☐ All digits are unique (e.g., `0x6` and `0xb` are different shapes)
- ☐ DIP switches to control the display are arranged so that each adjacent switch controls the next bit. (e.g., the switch for bit 0 is next to the switch for bit 1, which is next to the switch for bit 2, etc.)
- ☐ LEDs display the specified logic operations properly.

Excellence

- ☐ All digits are equally bright, regardless of the number of segments illuminated.

Verilog Structure and Style Specifications

Proficiency

- ☐ assign used to implement switch-to-LED logic in the top level module. (Note that it is standard practice to avoid putting 1 liner logic in a module; doing so would add more lines of codes than it saves!)
- ☐ Switch-to-7-segment logic contained in a module
- ☐ Switch-to-7-segment logic uses a case statement to select the correct segment pattern, and doesn't imply a latch
- ☐ Counter logic contained in a module
- ☐ Counter includes reset, enable and settable (possibly hardcoded) max count features. The max count feature sets the counter back to zero when the count reaches the max value.
- ☐ Counter is implemented using a single always_ff block.
- ☐ Top level consists only of instantiated modules and switch-to-LED logic.
- ☐ Descriptive filename that matches module name (e.g., `lab2_jb.sv`)

- ☐ One module per file with a descriptive name
- ☐ Descriptive variable names
- ☐ Neat formatting (e.g., standard indentation, consistent formatting for variable names (kebab-case/snake_case/camelCase/PascalCase))

Excellence

- ☐ Verilog parameters used to specify the width and maximum count values for the counter module

Simulation Specifications

Proficiency

- ☐ QuestaSim simulations carried out (possibly manually) for the 7-segment module.
- ☐ All simulations captured as legible waveform screenshots in report.

Excellence

- ☐ QuestaSim simulation with automatic testbenches for each 7-segment module covering all input-output pairs.
- ☐ QuestaSim simulation with automatic testbenches for the counter module. This simulation does not need to cover all possible states, but should show the reset, enable and max count features working correctly. These features may be captured in separate screenshots for legibility.
- ☐ QuestaSim simulation with automatic testbenches for the top module showing behaviors not-covered by module-level simulations: "are the connections to submodules correct?", "does the HSOSC work?" and "does the assign 1 liner work?".

Schematic and Block Diagram Specifications

- ☐ A schematic exists and a good faith effort has been made to meet the full specifications below (they are not yet in full effect, brace yourself for lab 2).
- ☐ A block diagram exists and a good faith effort has been made to meet the full specifications below (they are not yet in full effect, brace yourself for lab 3).

Other Documentation

Proficiency

- ☐ Calculations provided to demonstrate that the current draw for each segment in the seven-segment display is within recommended operating conditions.

Excellence

- ☐ No errors in LED current calculation (correct VON selected for current level, VON included in calculation, etc.).

Lab Writeup

Proficiency and Excellence

- ☐ Documentation embedded in a well-structured, concise report with one section per major deliverable. Sections should match structure of other specs.
- ☐ Spoiler tags are used to hide screenshots and code. Some unspoilered entries (~1 waveform, essential code snippets) allowed if they are essential to the narrative, kept to a minimum.
- ☐ Writeup contains minimal spelling or grammar issues and any errors do not significantly detract from clarity of the writeup.
- ☐ Statement of whether the design meets all the requirements. If not, list the shortcomings.
- ☐ AI prototype attempted and some reflection is recorded.
- ☐ Number of hours spent working on the lab are included.
- ☐ (Optional) List comments or suggestions on what was particularly good about the assignment or what you think needs to change in future versions.

FOR REFERENCE ONLY (NOT YET IN EFFECT)

Schematic Specifications

Proficiency

- ☐ All pin names labeled
- ☐ All pin numbers labeled
- ☐ Crossing wires clearly identified as junction or unconnected
- ☐ Neat layout (e.g., clear organization and spacing)
- ☐ All parts labeled with part number
- ☐ All component values present

Excellence

- ☐ Standard symbols used for all components where applicable
- ☐ Signals "flow" from left to right where possible (e.g., inputs on left hand side, outputs on right hand side)
- ☐ Title block with author name, title, and date

Block Diagram Specifications

Proficiency

- ☐ Each module is represented by a block diagram
- ☐ Bare logic in all module is represented by appropriately drawn gates.
- ☐ Submodules in each module are represented by blocks inside of the instantiating module.
- ☐ Submodules have all ports represented by pin symbols on the boundary of the submodule, each with a port name.
- ☐ Submodules indicate the name of the module being instantiated and the name of the instance.
- ☐ All connections between module ports, logic and submodules are indicated.
- ☐ Module ports are represented by pin symbols on the boundary of the module and labeled with port names
- ☐ All nets internal to the module are labeled, even when they share a name with a port on a module/submodule boundary.

Excellence

- ☐ Appropriate use of bus notation for multi-bit signals (e.g., `data[7:0]` for an 8-bit bus), including fan-in and fan-out when needed.
- ☐ Appropriate use of implicit connections (i.e.: connect-by-label-name) to reduce routing connection
- ☐ Block diagram is an exact, 1:1 representation of the Verilog code.